CHAPTER 9

Beam Diagnostics

9.1 Beam Position Monitors

The Tevatron Beam Position Monitor (BPM) readout electronics and software system consists of 960 channels of electronics to process analog signals from 240 BPMs, front-end software, online and controls software, and the T39 ACNET interface. The system reads signals from both ends of the existing directional stripline pickups to provide simultaneous proton and antiproton position measurements.

BPM Pickups

The pickups in the Tevatron ring are part of the superconducting quadrupole assemblies. Each BPM is a pair of 50 Ω striplines 18 cm long, each subtending 110 degrees of arc, with a circular aperture of 7.0 cm diameter. Each BPM measures either the vertical or the horizontal coordinate, and there are approximately 240 BPMs situated around the Tevatron ring. The pickups are directional (26dB), and are read out on both ends. Special half-length BPMs are installed near the B0 and D0 interaction regions.

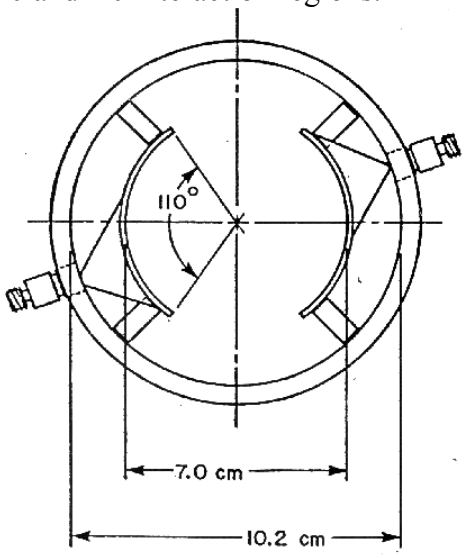


Figure 9.1 : Tevatron BPM and Specifications

Key Specifications (Protons)*:

Measurement Range: ±15mm

Absolute Position Accuracy: < 1.0 mm

Long Term Position Stability: < 0.05 mm

Best Orbit Position Resolution: < 0.02mm

Position Linearity: < 1.5%

Relative Position Accuracy: < 5%

Intensity Stability: < 2%

Key Specifications (Pbars)*:

Measurement Range: ±15mm

Absolute Position Accuracy: < 1.0 mm

Long Term Position Stability: < 0.05 mm

Best Orbit Position Resolution: < 0.05mm

Position Linearity: < 1.5%

Relative Position Accuracy: < 5%

Intensity Stability: < 2%

** All values are 3σ*

Electronics and Signal Processing

The 53 MHz component of the BPM pickup response is used to measure beam positions. A schematic of the signal processing path is shown in Figure 9.2. Signals from the BPM pickups in the Tevatron tunnel are carried over foam RG-8 coaxial cables to the electronics system in one of 27 service buildings situated on the surface above the ring. Each VME subrack contains a Motorola processor module, a timing board providing clock and interrupt signals, front-end analog filter boards providing 53 MHz bandpass filtering and signal attenuation, and 8-channel 80 MHz digital signal receiver boards. All interconnections are made using double-shielded coax cables. A photograph of a completed and installed VME subrack is shown in Figure 9.3.

The digital receiver board is very similar to those used for the Recycler BPMs and identical to boards acquired for the Main Injector and P1 transfer line BPM upgrades. The digital signal receiver board consists of a 14-bit A/D converter, digital down-converter, FPGA (Field Programmable Gate Array), RAM, and VME interface. Signals are synchronously digitized at 74 MHz. Narrow-band (about 1 kHz) and wide-band (47 kHz) digital filters provide closed-orbit (CO) and turn-by-turn (TBT) measurements.

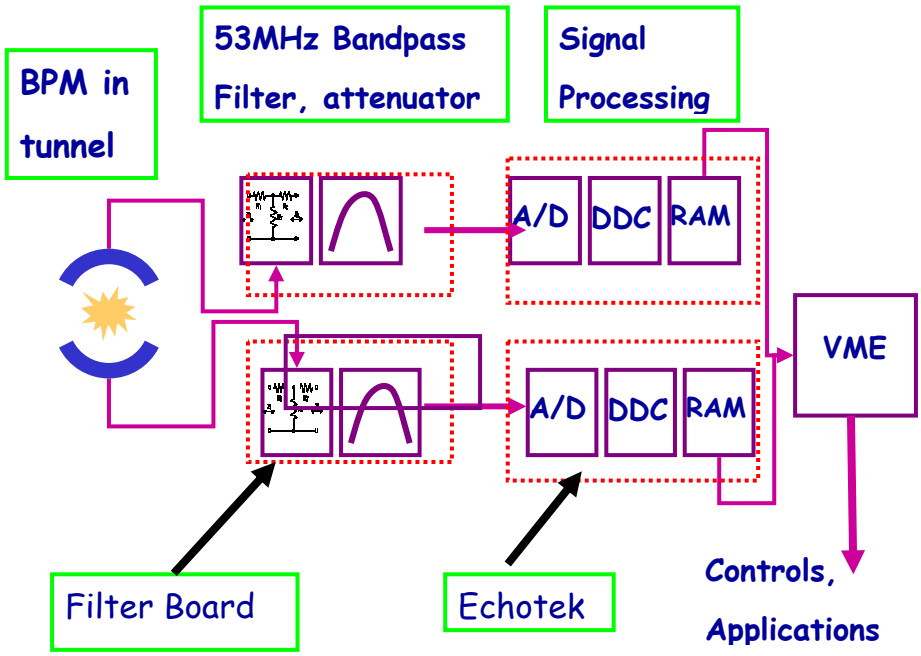
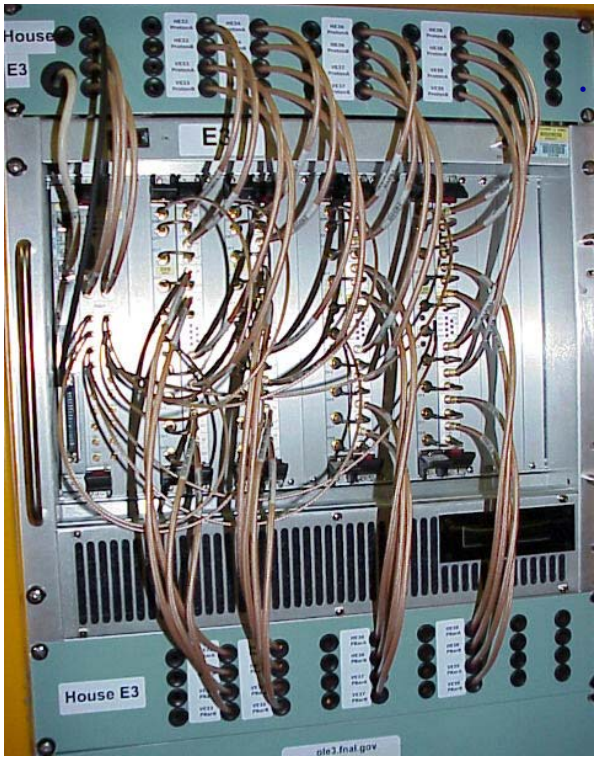


Figure 9.2: Tevatron BPM signal processing path.



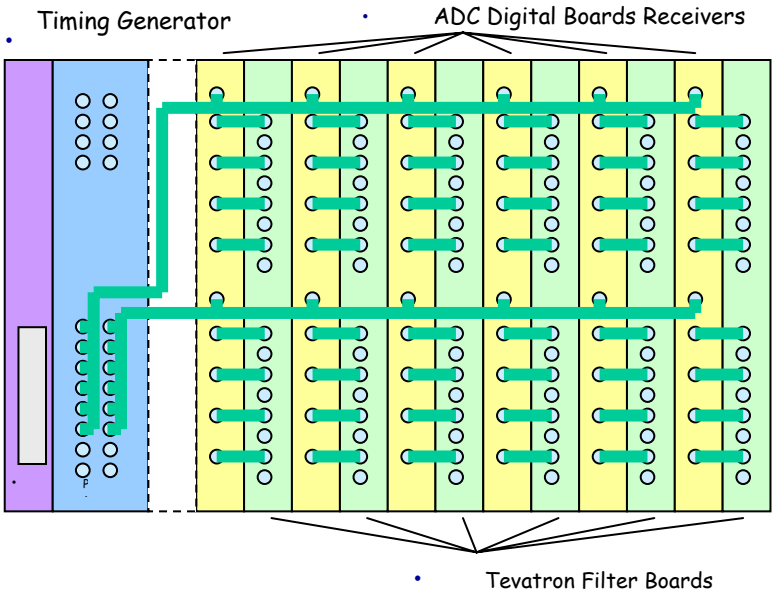


Figure 9.3: Completed VME subrack in the E3 service building and crate layout.

Closed Orbit

Transverse positions are computed using the following formula:

$$P = 26^* (|A| - |B)|/(|A| + |B|)$$

where *A* and *B* are the BPM response from the two plates and 26 is the scaling factor to convert from BPM response to position (in mm) for this pickup geometry.

An example of the performance of the system can be seen in Figure 9.4. In this figure the difference in proton positions at each BPM at 150 GeV for two stores are shown. Orbit oscillations of about 100 μm are seen.

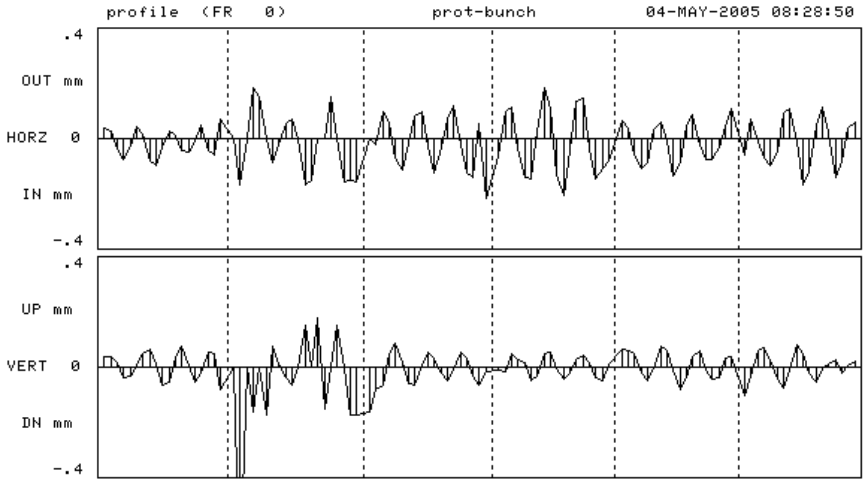


Figure 9.4: Horizontal (top) and vertical (bottom) orbit differences between two stores, measured at 150 GeV. Vertical scale is +- 400 μm.

Antiproton Position Measurements

The antiproton beam positions are determined by a "deconvolution" technique that subtracts the proton signal contamination on the antiproton pickup. This subtraction is required because of the imperfect directionality of the pickups. The subtraction is implemented using the following formulas:

$$A'_{Pbar} = A_{Pbar} - aA_P - bB_P$$
$$B'_{Pbar} = B_{Pbar} - cB_P - dA_P$$

The coefficients *a, b, c, d* are determined empirically. The coefficients depend on the beam position in the pickup so it is important to determine these at the beginning of every store. The proton and antiproton positions at the beginning of a proton-pbar store are shown in Figure 9.5 (after deconvolution).

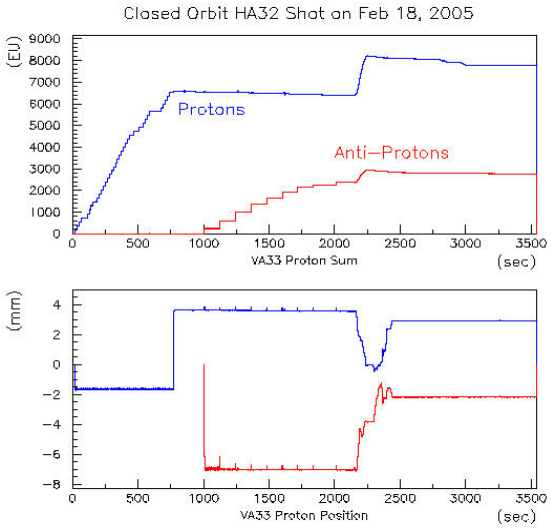


Figure 9.5: Top plot: proton and antiproton sum signals. Bottom plot: Antiproton position (bottom curve) during injection and beginning of collisions.

Turn by Turn Measurements

The BPM system provides TBT measurements at beam injection and on request. The system provides 8192 turns of data. An example of TBT measurements on injection can be seen in Figure 9.6, showing synchrotron oscillations.

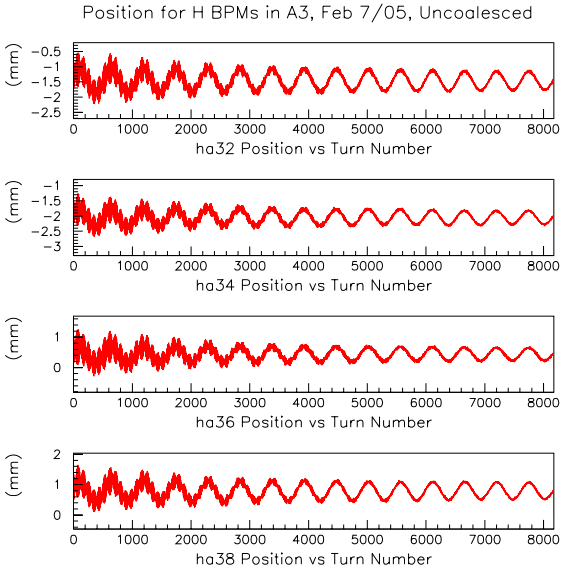


Figure 9.6: Proton position at 4 locations during the first 8192 turns after injection into the Tevatron.

9.2 Beam Loss Monitors

The BLM readout system is designed to perform several tasks: to provide a flexible and reliable abort system to protect Tevatron magnets; to provide loss monitor data during normal operations of the Tevatron; and to provide detailed diagnostic loss histories when an abort happens. Beam losses are detected using ion chambers.

The basic principle of operation of the new BLM system is to integrate for a short period of time, typically 21 μs, and digitize to 16 bits. There are two integrators per channel, running in a "Ping-Pong" mode, alternating between charge integration and digitization, so that no loss is missed. While one channel is integrating, the other is digitized, its integrator is reset, and the data are processed. The reset and processing time set a lower limit of 15 μs. The digital data are used to construct several numbers that are compared against thresholds to generate abort signals. These constructed data are sliding sums, which are a measure of the integrated loss over a variety of time scales from a single reading to the integrated loss over a period of up to 64k cycles. The abort signal is made in firmware by looking at these sums and thresholds as well as the number of channels requesting an abort.

The system uses a standard VME format crate. Besides the VME crate computer in Slot 1 that communicates data to the main control system, the BLM system includes five types of custom cards:

- Digitizer Cards (DC)
- Timing Card (TC)
- Control Card (CC)
- High Voltage card (HV)
- Abort Card (AC).

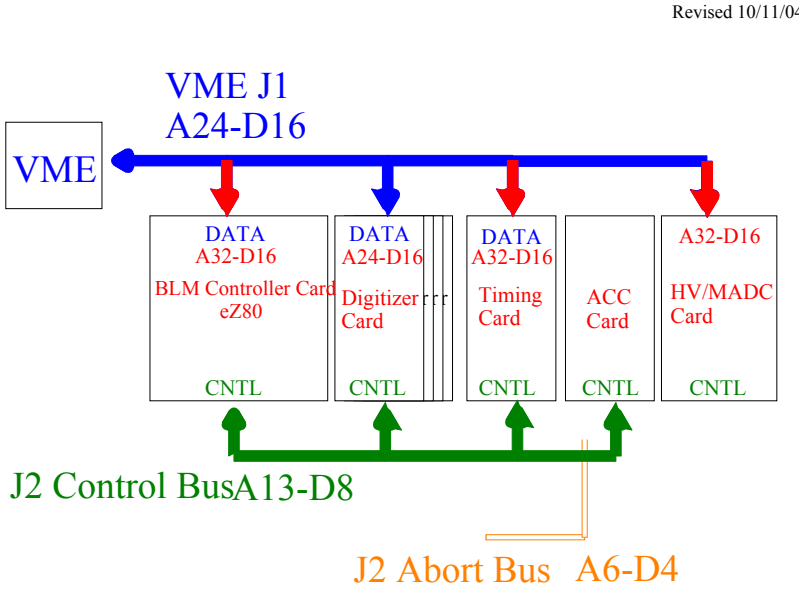


Figure 9.7: Block diagram of a BLM crate

A custom J2 backplane is used for local system communication. A Control Bus using the user-defined pins on the J2 VME connector handles all of the critical BLM controls. This

bus has 13 address lines and 8 data lines. The Controller Card is the only master on this bus, and the other cards are slaves. Also on the J2 connector is an Abort Bus where the AC is the master and the digitizer cards are the slaves.

The sliding sum time scales and corresponding buffers and abort channels are referred to either by the sum (or abort number) or intended time scale. These are as follows:

Number	Name	Typical Time Scale	Circular Buffer Depth
0	Immediate	20 μs	64kB
1	Fast	1 ms	16kB
2	Slow	50 ms	4kB
3	Very Slow	1 s	4kB

In this document, we include a summary description of each of the components followed by a description of the bus and communications protocol and detailed descriptions of the functions performed by each module including address maps.

Digitizer Card

The Digitizer Card (DC) integrates and digitizes the current from four loss monitor chambers each beam revolution. To avoid dead time between measurements, signals for each input are switched between the two channels of an integrator chip. Results are digitized from the two channels on alternate cycles and fed to on-board programmable logic devices.

The digitizer has a 16 bit resolution. Scaling is such that one digitizer count represents 15.26 fC (femto Coulombs) of charge in the integrator. The sensitivity of the BLM ion chamber is approximately 70 nC of charge per Rad.

The logic maintains three running sums per channel with programmable durations of up to 65,536 base clocks (1.4 seconds for the Tevatron) and compares the current measurement and the running sums to abort thresholds (4 thresholds in all). Each threshold can be set independently for each channel. There can be up to 15 digitizer cards in a crate.

The block diagram in Fig. 9.8 illustrates the signal processing for each channel. Note that the Sum registers will be read and the Threshold Registers written over the BLM Control Bus. The SRAM memory which stores the integrator output values can be read over the VME bus (J1) by the crate computer.

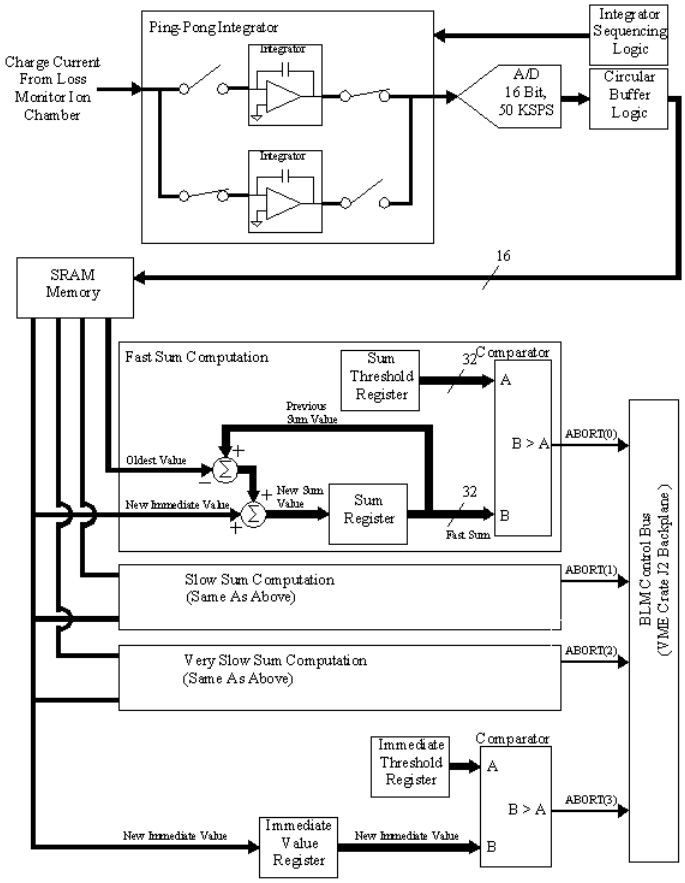


Figure 9.8: Block diagram of the signal processing for one of the four channels on the Digitizer Card.

Timing Card

The Timing Card (TC) receives accelerator system-wide timing information from three sources, the Tevatron Clock (TCLK), the Beam Sync Clock (BSYNC) and Machine state Data (MDAT).

The TC decodes BSYNC to generate the BLM system master clock which it distributes on the BLM Control Bus. This will be generated from the AA marker with a 21μs period. The master clock signal is known as *Make_Meas* ("Make Measurement").

The TC maintains a 64k circular buffer of timing information for each cycle including a 32-bit Unix time (seconds since 1970) and a 24-bit microsecond counter which is reset at one second intervals; this buffer is in parallel with the circular buffer of loss measurements in the digitizers. The master clock defines the integration interval of the digitizers and sets the threshold-comparison timing and abort-logic comparison timing. The TC also generates signals at appropriate intervals to cause the digitizers to latch the current values of the sliding sums and the Controller Card to read these sums with the latched timing information.

The TC decodes TCLK and sends a signal to freeze the data buffers in the Control card, Timing Card and Digitizers in the case of an abort. Other events from TCLK are used to

signal the BLM system to collect and store synchronous ring-wide data samples for beam studies. The MDAT signal is decoded to determine the machine state and generate an interrupt to the Control Card causing it to load the appropriate abort thresholds and logic when the Tevatron machine state changes.

Control Card

To ensure that data communications and other tasks running on the VME crate computer do not impact the reliability of the BLM abort logic, the Control Card (CC) provides an independent dedicated processor that manages the setting of abort thresholds and other parameters used in the abort logic. The Control Card CPU is a 24-bit address, 8-bit data, 50 MHz microcontroller. The CC communicates with the other system cards over the dedicated custom J2 backplane keeping local communications separate from VME data transfers. The CC also maintains circular buffers that store the histories of the three running sums for each digitizer channel with time stamps provided by the TC. The histories will be at least 4096 time bins deep. The history can be read out via VME either on command from VME crate computer or saved in response to an accelerator control signal. The CC also stores abort thresholds for each of the sums for each channel for up to 256 machine states.

When a change in accelerator state is detected, the CC updates the thresholds in the digitizer cards as well as the abort masks and multiplicity requirements in the Abort Control Card.

HV Card

The High Voltage card is a double-wide 6U high VME module that can carry one to four high voltage modules that are independently controlled through the VME bus. It has an 8-bit switch selectable card number which sets the card address corresponding to VME address. A quad 12-bit DAC provides the program voltage for each of the high voltage modules for voltage output control. The combination multiplexer and 16-bit ADC reads the high voltage monitors for each module.

The card incorporates an FPGA (Field Programmable Gate Array) to interface with the VME bus, local timing and control. The FPGA receives all the VME bus control, address and data lines for read/write of data on the card. The FPGA can be programmed from the front panel through the Active Serial Program connector.

The program voltage circuitry consists of a 12-bit four-channel DAC device and an op-amp gain circuit. The DAC is controlled from the VME bus through an FPGA to select and send data to the selected channel. The DAC accepts straight binary which corresponds to a program voltage output of 0 to 10V. The high-voltage is linear in the setting value with a maximum value of 2250 V.

To read all the high voltage monitors, the card uses a 16-to-1 multiplexer and 16-bit unipolar input digitizer. The circuit operates in a circular mode, such that the digitizer continues digitizing all the monitor signals from each channel and storing the data into registers. The registers then can be read at anytime through the VME bus. The ADC has an input range of 0 to 3.33V with an output of straight binary. The timing and control is done through the FPGA.

The High Voltage module is a self-contain module with two SHV connectors, one for high voltage output, the other for a high voltage return. A third connector is used as an I/O for input power, program voltage and high voltage monitoring. High voltage is produced by a dc to high voltage converter that is controlled by a programmed voltage input. The high voltage output is regulated and has low ripple output. The module also has three high voltage monitors for voltage output, voltage input return and current output monitoring. Shown below are the specifications for the module.

Abort Card

The four abort signals from each channel on each digitizer card are read by the Abort Card (AC) every integration interval. The aborts of a particular type are counted and compared to a programmable multiplicity requirement for that abort type. It is possible to mask channels off in the AC so they do not participate in the count. If the multiplicity for that integration interval equals or exceeds the threshold, a beam abort signal is generated. This logic is illustrated in Fig. 9.9. To accommodate the different operating conditions, the abort masks and multiplicity thresholds in the Abort Card can change depending on the machine state. We have also included a serial link on the Abort Card to allow a single point to receive information from all the BLM crates around the ring to be able to implement a ring-wide abort condition

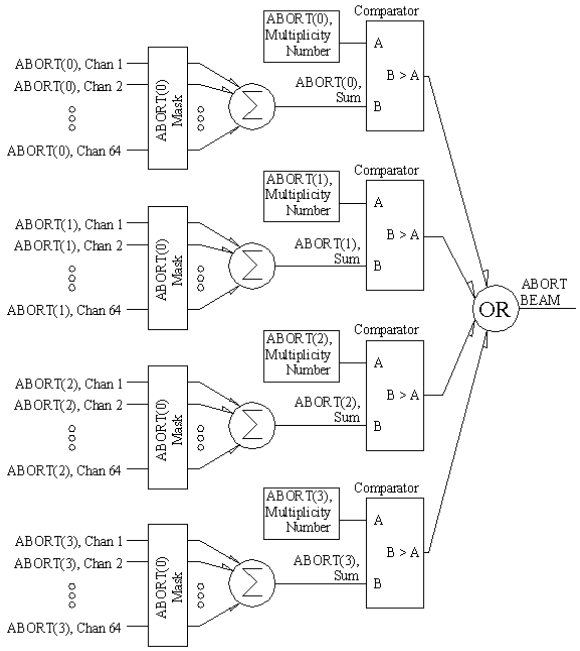


Figure 9.9: Abort Card multiplicity logic.

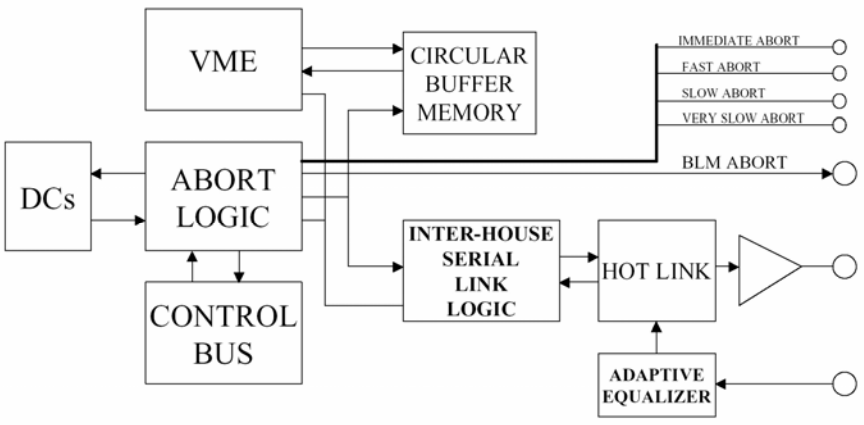


Figure 9.10: Overview of Abort Card functions.

Chassis

The chassis is an integrated 6Ux160mm VME crate, power supply and fan. In addition to the J1 backplane, each crate includes a custom J2 backplane that handles the BLM control bus with all lines bussed on the A and C rows for slots 4-21. Slots 1-3 will have no backplane connections on rows A and C. Row B includes the standard extensions for VME operation. The power supply blocks the rear of the backplane, so transition modules cannot be used in a BLM crate. The fan tray also provides an interface to allow slow control and monitoring via Ethernet.

Turn-by-Turn Buffers

In addition to the diagnostic buffers maintained by the Controller Card, which are circular buffers that are periodically overwritten, the BLM system has two linear buffers in the digitizer that are triggered and are not automatically overwritten. These buffers are Turn-By-Turn (TBT) and are each 8 kB. The TBT buffers are designed to allow the simultaneous sampling of beam position in the BPM and beam losses in the BLM.

The injection TBT buffer (ITBT) is designed to match the BPM injection TBT buffer and is triggered by ITBT Trig. The studies TBT buffer is designed to match the BPM TBT buffer used for beam studies. The STBT is triggered by STBT_Trig, both of these triggers are generated on the TC by clock events on TCLK or BSCLK. When either of these TBT buffers is triggered, the digitizer cards and timer card will set a bit in a status register indicating the TBT operations are in progress and that the TBT memory is not accessible from VME. Once the TBT operation completes, or if an abort happens, the digitizer cards and timer cards will reset the status bit, and VME will have access to the TBT memory.

Once it has been triggered, the ITBT will fill to its limit of 16k and stop. It will not be overwritten until another injection clock event happens. If another ITBT_Trig happens, prior to the completion of the ITBT operation, the ITBT pointer will be reset to 0, and

16kB of new TBT data will be written into the ITBT buffer. Only the first 8kB are protected from an STBT_Trig.

The STBT buffer once triggered, will fill to the limit of 16kB and stop. It will not be overwritten until another studies clock event happens. If another STBT_Trig happens, prior to the completion of the STBT operation, the STBT pointer will be reset to 8kB and 8kB of TBT data will be written into the STBT buffer.

Revised 10/11/04

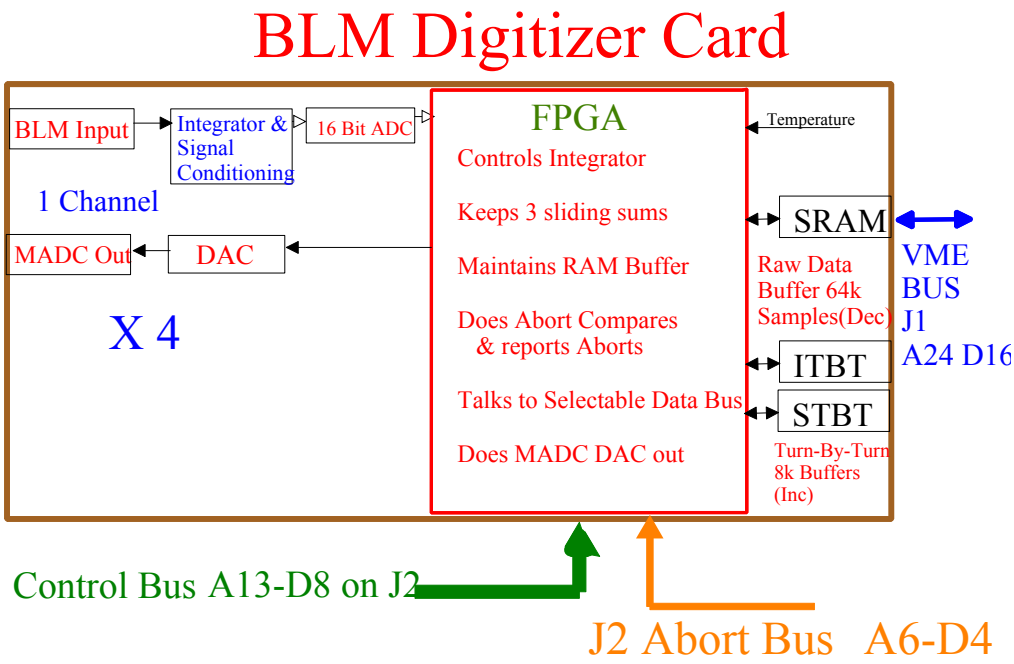


Figure 9.11: Digitizer Card functions

BLM Crate Normal Operations Sequence

Once the settings are loaded into the TC, DCs and AC, the system is ready to run. The BLM operations are initiated by a clock event such as "Prepare for Beam" which will cause the TC to issue a Digitizer Card Reset (*DC_Reset*) on the control bus. The *DC_Reset* causes the DCs to zero all sliding sums and causes the DCs and the TC to set all circulary buffer pointers to FFFF. This assures that all buffers are synchronized and ready to take data.

The primary clock for the BLM system, *Make_Meas*, is derived from the AA marker on the beam sync clock (typically 21 μs). *Make_Meas* is transmitted on the BLM control bus to all BLM cards. Optionally the *Make_Meas* signal can be created by dividing the AA marker or by dividing down an internal clock. The shortest allowable period for this signal is 15 microseconds due to the reset time needed by the integrators.

On the digitizer cards the *Make_Meas* signal defines the sample period, causing the integrators to switch between channels for each input and triggering the ADCs to digitize

the charge for the channel not being integrated. After that, the sliding sums are updated and all abort comparisons are made. At this time the new ADC readings are written to a 64kB circular buffer which is used for diagnostic purposes as well as the source of the sliding sums. The new ADC data may also be written to one of two turn-by-turn (TBT) dedicated studies buffers. The abort states are latched on the next *Make_Meas*. Thus the DC has the full sample period to do its conversions, make the sliding sums and do the abort compare with thresholds. The timing card stores real-time clock data on each cycle in a 64kB circular buffer that is synchronized with those of the digitizers.

On the AC, the *Make_Meas* signal causes the abort summing state machine to cycle through each BLM channel by putting the channel address on the abort bus and to read back from each channel the state of each of its abort requests. For each abort type, each channel has an abort mask bit which determines if that channel is allowed to request an abort of that type. A count is made for each of the four abort types of allowed AND requesting channels (i.e. those above threshold). If the number of channels requesting an abort for any of the four abort types equals or exceeds the abort multiplicity setting for that abort type, an abort request is transmitted from the card on a 50Ω TTL line driver.

The *Make_Meas* signal, therefore, causes the data to be taken and the abort logic to be updated every cycle. While a sliding sum might be the sum over 500 samples (10 ms) its abort threshold is compared every 21 μs.

During each 21μs cycle, the digitizer cards make and update the three sliding sums of samples. These sliding sums are compared every cycle to their abort limits. However, for diagnostic purposes, these sums are stored periodically in circular buffers on the Control Card. This process is controlled by the TC, which periodically generates 3 latch signals, one for each sliding sum. The latch signals cause the DCs to latch the appropriate sum and the TC to latch the time stamp and to interrupt the CC so that it knows the data is latched and ready to be read and stored in the appropriate circular buffer. The individual ADC readings are 16 bits; however, the sliding sums are 32 bit numbers. Therefore, the dynamic range of, for example, the 1 second sliding sum is almost 32 bits. These sliding sums are the total integrated loss over the sum interval, not just samples of losses spaced in time.

At any given time, the BLM has a variety of stored loss histories with different time resolutions: the 64kB raw measurement buffer provides 1.4 seconds of loss data with 21 μs resolution; the 16kB fast circular buffer provides 16 seconds of integrated loss data with 1 ms resolution, the 4kB slow circular buffer provides 200 seconds of integrated loss data with 50 ms resolution; and the 4kB very slow buffer provides 4096 seconds, over an hour, of integrated loss data with 1 second resolution. As one can see, in the event of an abort, there is a very detailed history of losses prior to the abort, which may be examined to aid in diagnosing the problem.

9.3 Sampled Bunch Display

9.4 Fast Bunch Integrator

9.5 SyncLite and Abort Gap Monitoring

During operation of the Tevatron in colliding beam mode, a small amount of the beam diffuses out of the bunches and spreads around the ring. The presence of beam in the abort gap can have a serious effect on superconducting magnets and a devastating effect on the silicon detector of CDF. During an abort, the kicker magnets ramp up during the abort gap. Beam passing through the kickers while they are ramping sprays into magnets and into the silicon detector. There are 2 methods for directly measuring the beam in the abort gap using synchrotron light: CID camera, and photomultiplier tube.

Theory

A charged particle that undergoes transverse acceleration emits radiation in a cone around its velocity vector. This radiation is called synchrotron radiation after its first observation in a synchrotron. The Tevatron has 1113 RF buckets and typically contains 10^{13} protons in 36 bunches arranged in 3 trains of 12 (the antiproton intensity is ~1/10 the proton intensity).

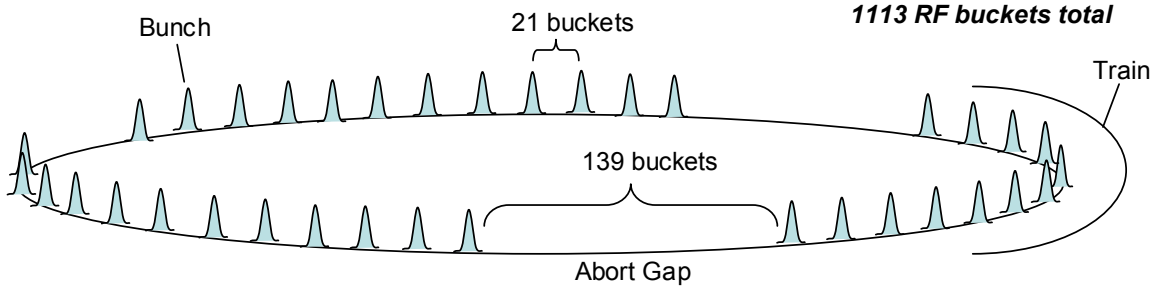


Figure 9.12: Bunch spacing in the Tevatron

Apparatus

Figure 2 shows the optics of the synchrotron light apparatus which is located near the short warm section at C11.

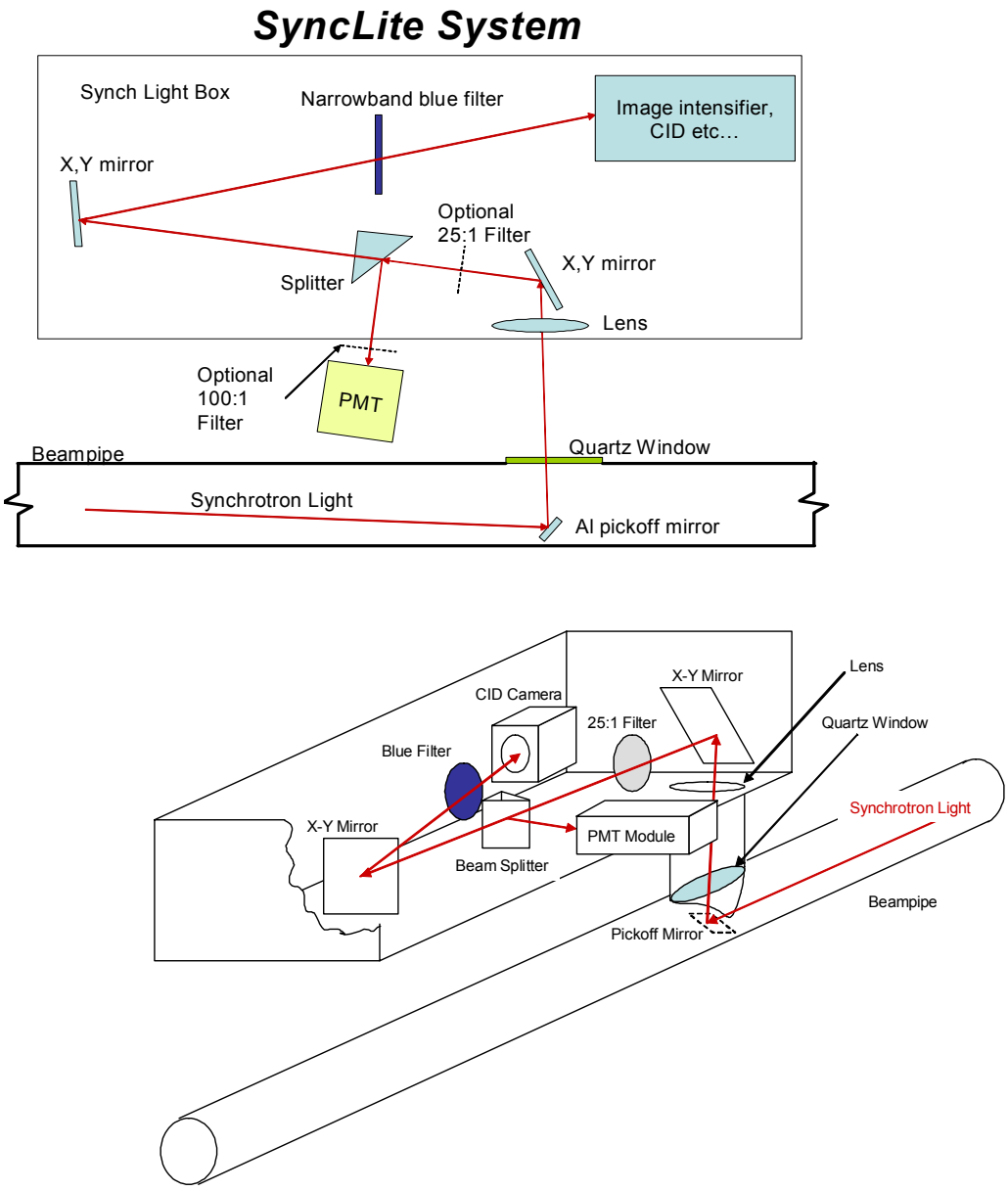


Figure 9.13: Diagram of SyncLite system. The optics through the beam splitter are shared by both the camera and PMT systems. The top drawing is the logical diagram and the bottom drawing is the physical layout (100:1 filter is in PMT module).

The light is picked off by a mirror in the beam pipe and directed out a quartz window to the light box. Inside the light box, the light traverses a 1500mm focal length lens and another mirror before hitting the beam splitter. The synchrotron light is clearly visible on the wall of light box in Figure.

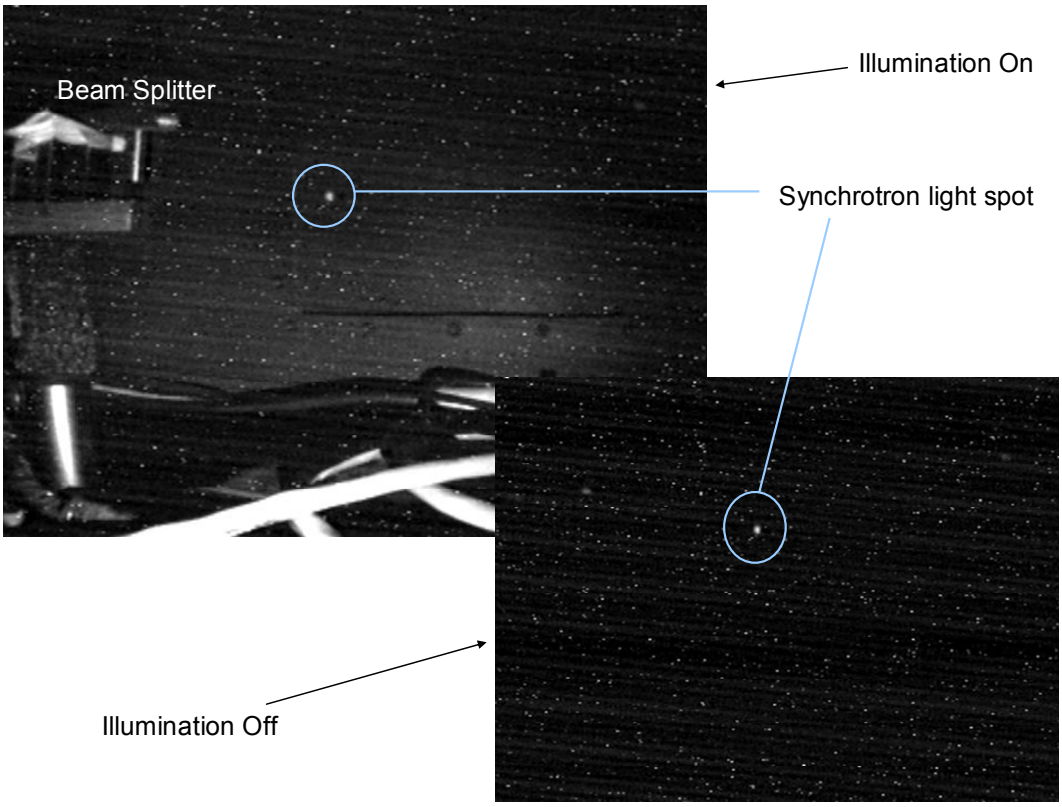


Figure 9.14: Video stills from a CCD camera mounted in the light tight box showing synchrotron light impacting the side of the light tight box. The smaller white specs are radiation damaged pixels.

After the beam splitter, the PMT system and camera system follow separate paths. Just before the beam splitter there is a 4% neutral density filter that can be inserted into the light path to facilitate calibrations.

The observed number of photoelectrons is tabulated as follows:

	Optical efficiency through beam splitter	**Optical efficiency after beam splitter**	**Wavelength acceptance**	**Photocathode quantum efficiency**	**photoelectrons / 10^9 protons / bucket**
PMT System	0.34	–	100 nm	0.14	0.1
CID System		0.92	20 nm	0.12	0.015

CID and Camera Version

Every pixel in a CID array can be individually addressed via electrical indexing of row and column electrodes. Unlike Charge Coupled Device (CCD) cameras which transfer collected charge out of the pixel during readout (and hence erase the image stored on the sensor), charge does not transfer from site to site in the CID array. Instead, a displacement current proportional to the stored signal charge is read when charge "packets" are shifted between capacitors within individually selected pixels. The displacement current is amplified, converted to a voltage, and fed to the outside world as part of a composite video signal or digitized signal. Readout is non-destructive because the charge remains intact in the pixel after the signal level has been determined. To clear the array for new frame integration, the row and column electrodes in each pixel are momentarily switched to ground releasing, or "injecting" the charge into the substrate.

This principle of operation makes CID technology fundamentally different from other imaging techniques, giving rise to a number of technical advantages that can be used to solve imaging problems. For instance, the nondestructive readout capability of CID cameras makes it possible to introduce a high degree of exposure control to low-light viewing of static scenes. By suspending the charge injection, the user initiates "multiple-frame integration" (time-lapse exposure) and can view the image until the optimum exposure develops. Integration may proceed for milliseconds or up to several hours with the addition of sensor cooling, applied to retard accumulation of thermally-generated dark current.

CID sensors also offer wide spectral response, from 200 to 1100 nanometers, allowing capture of images produced by light sources ranging from UV to the near IR. And the PMOS structure reduces the effect of radiation on sensor operation, making CID's less vulnerable to disruption in low-level radiation environments than NMOS devices (structure used in many CCD's). Radiation hardened CID's are currently employed in nuclear power, industrial X-ray, scientific, and space applications.

Since each pixel in the CID array can be addressed individually, flexible readout and processing options are made possible. For example, "Progressive Scan" readout enables real-time processing by eliminating the delay required to combine odd and even fields (2:1 Interlace scanning). Instead, lines are read sequentially (1, 2, 3, 4, etc.) allowing an image processor to analyze the latest row of video information while readout continues to the next line. The 60 frame per second output of these cameras provides high-speed operation.

The SyncLite system functions by using a gated image intensifier to act as a fast shutter and amplifier for a generic CID (charge injection device) camera. This allows for the accumulation of many short-duration ‘frames’ during one 1/30 sec camera frame. The intensifier is operated at a gain of ~1000. The number of times the shutter is opened during a single camera frame is adjusted by the DAQ system based on the measured intensity. In the case of the abort gap, this is typically every 4^{th} turn (~12 kHz). A LabView DAQ system collects the camera frames and fits horizontal and vertical projections of the beam profile to obtain the integrated intensity. Each abort gap measurement is the sum of 200 camera frames, or 8×10^4 abort gaps. Camera data of the abort gap are displayed in Figure 4 and Figure 5. The bump corresponds to a DC beam intensity around the ring of ~5 E9.

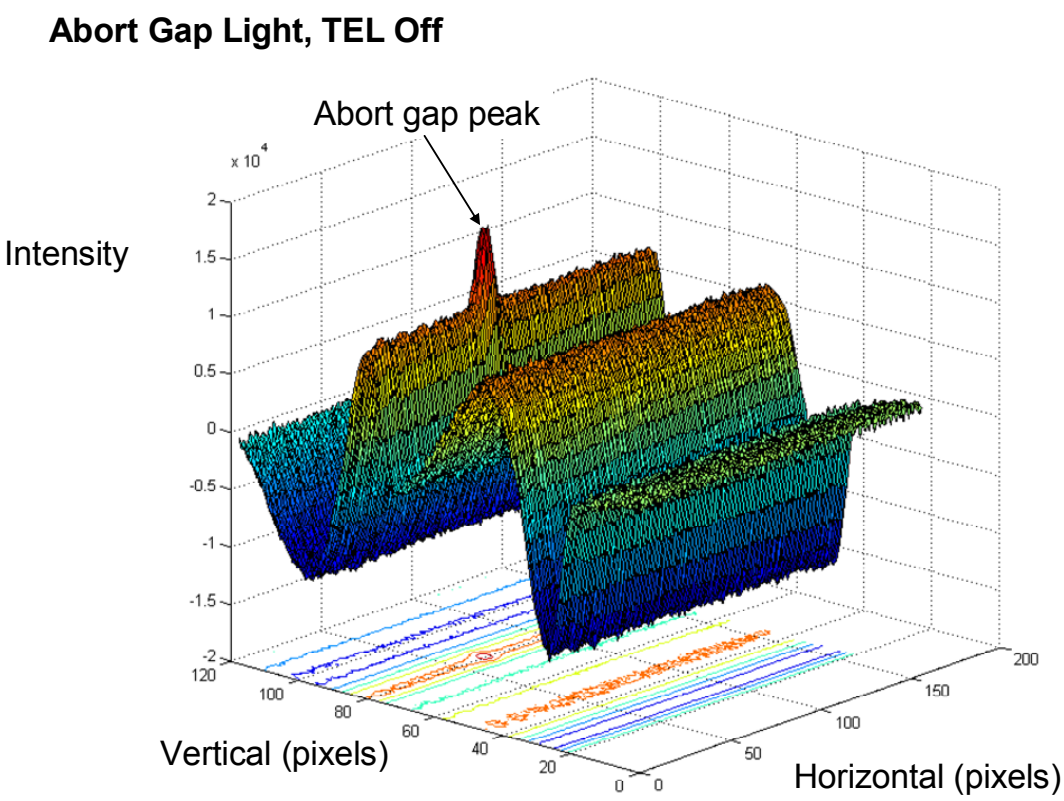


Figure 9.15: Camera image in abort gap. This is after pixel by pixel background subtraction, but before horizontal line subtraction. The peak corresponds to a DC beam intensity of ~5 E9.

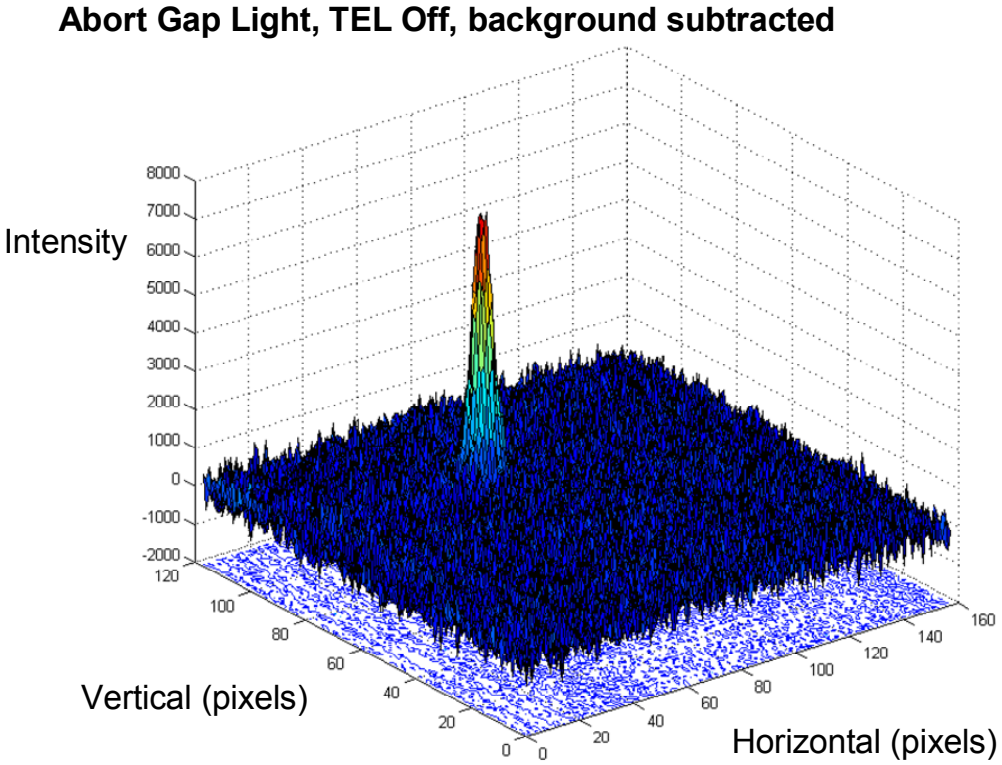


Figure 9.16: This image is after both pixel and horizontal line subtraction. The peak corresponds to a DC beam intensity of ~5 E9.

Photomultiplier Version

A 9-stage side window photomultiplier tube is attached to the SynchLite optics box and observes the light from the beam splitter. Between the beam splitter and the PMT, there is a 1% neutral density filter which can be moved in or out of the light beam.

Gated PMT

To avoid saturating the PMT with the light from the main bunches, there is a gating circuit attached to 2 of the dynodes of the PMT. The gating circuit holds the dynodes at a potential below the previous dynodes effectively turning off the tube (Figure 6). When the gate is on, the dynodes are pushed up to their nominal operating voltage.

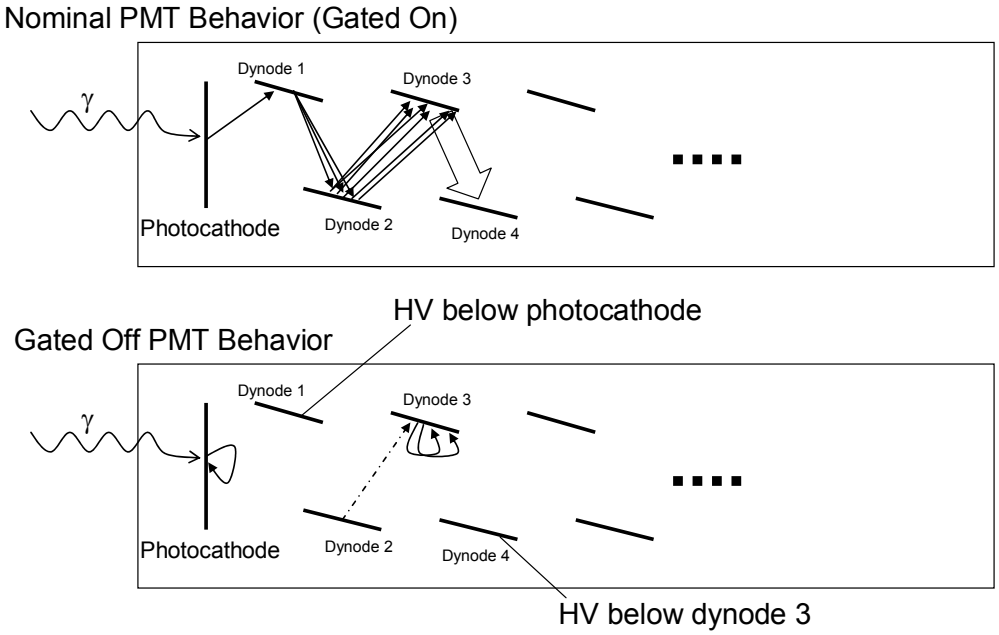


Figure 9.17: PMT behavior for gated on and gated off modes. The gated on mode looks like an ordinary PMT, while the gated off mode turns around the field lines between several dynodes effectively shutting off the multiplication.

Data Acquisition

The DAQ system consists of an MVME board running VxWorks talking to a COMET 12-bit ADC board and a VRFT board for beam timing. The PMT anode signal is brought upstairs to a fast integrator which feeds the ADC board. The integration gate is typically 1.4 microseconds (2/3 of the abort gap). The DAQ program on the MVME performs a ~60ms readout cycle once every second (1000 samples of each abort gap). Figure 7 and Figure 8 show the timing of the gating for a number of turns. Only one gate happens every turn, so over 3 turns each abort gap is sampled once.

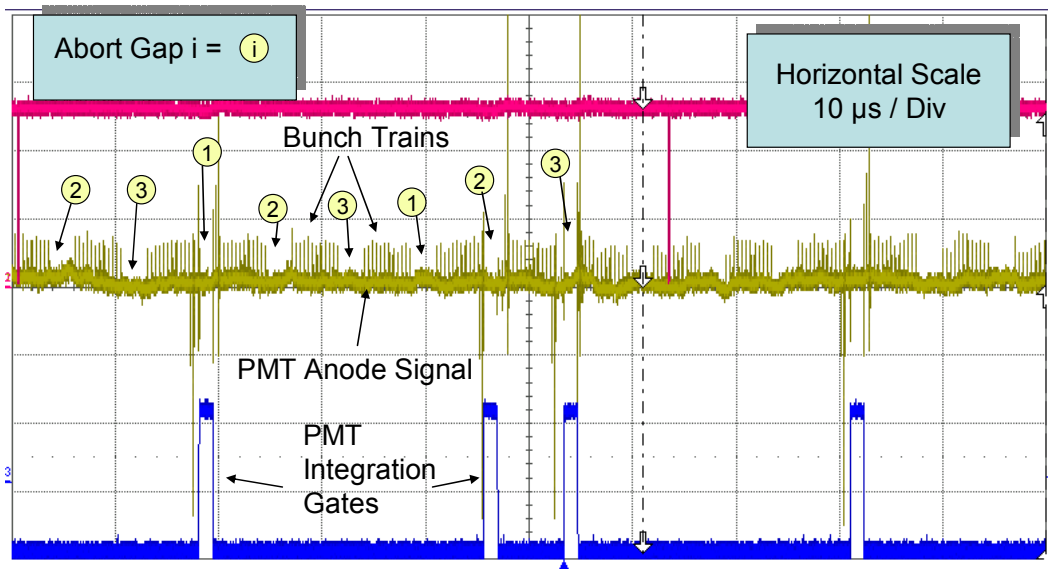


Figure 9.18: Scope trace showing timing of PMT gates. The anode signal is into 50Ω and is displayed on a 2mV scale. The first gate from the left occurs at abort gap 1. The second gate is abort gap 2, one and one third turns later, and the third is abort gap 3. The spacing between gates is necessary to keep the duty cycle low enough for the gating circuit.

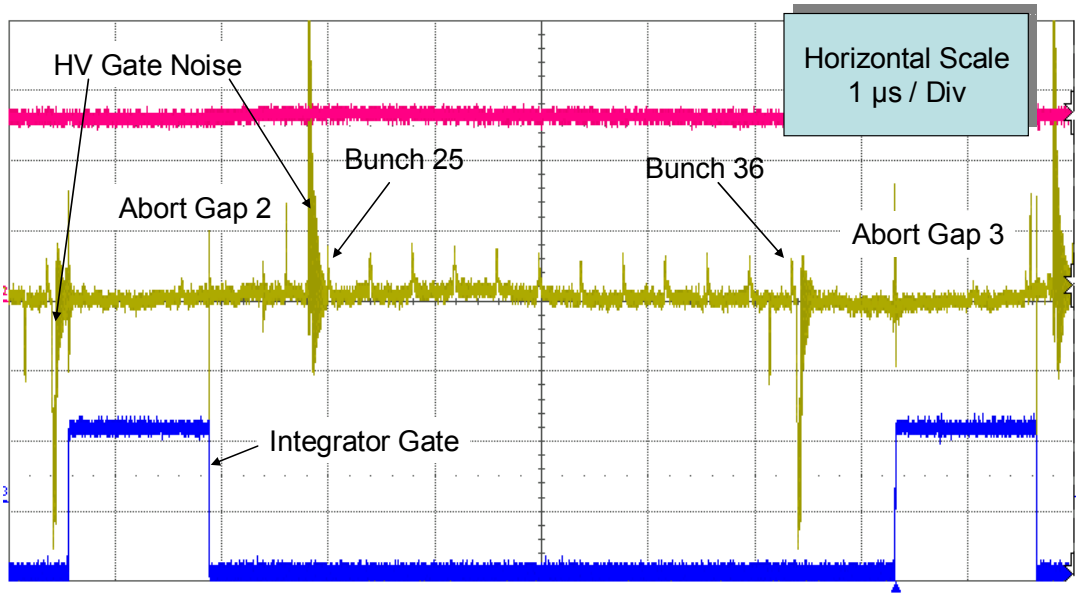


Figure 9.19: Zoomed view of Figure . Each abort gap has a different portion of it sampled, i.e. abort gap 1 is gated in the middle, abort gap 2 is gated at the beginning, and abort gap 3 is gated at the end.

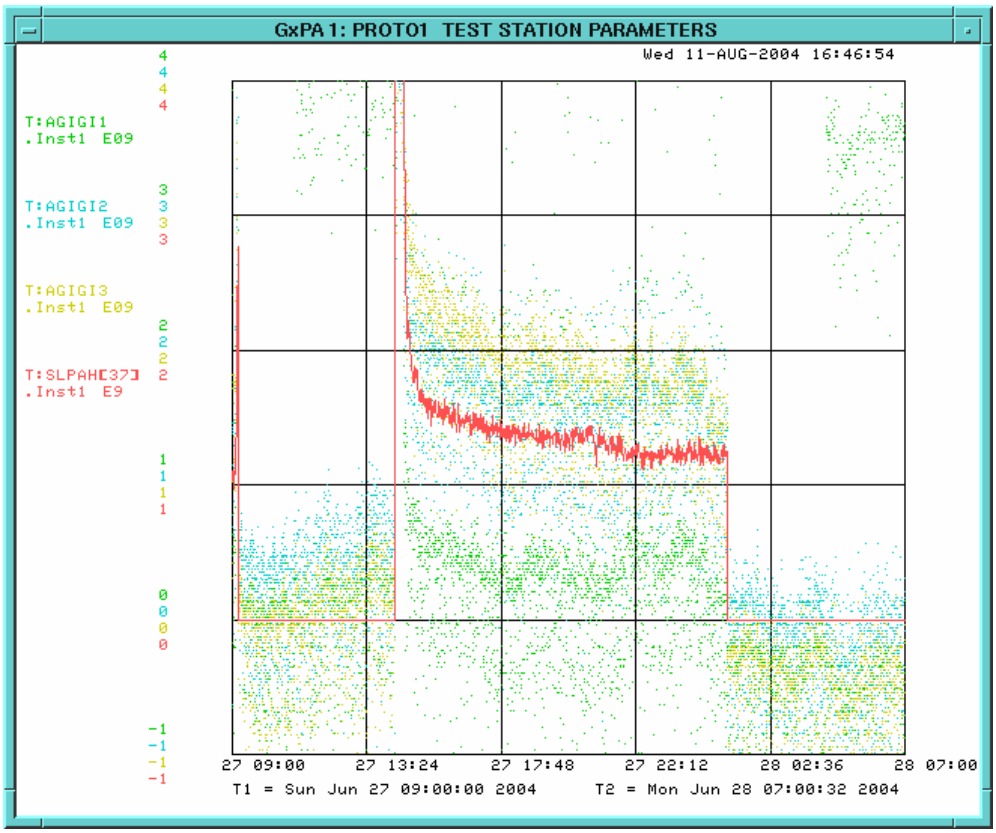


Figure 9.20: Plots of both the PMT and the SynchLite system. The PMT system is the AGIGIx devices. The SynchLite system is the SLPAH device. One can see the shift in backgrounds for the PMT system before and after the store.